IN THE CLAIMS:

Claim 1 (Currently Amended): A method of manufacturing a code address memory cell, the method comprising the steps of:

forming a gate insulating film in which a plurality of oxide films and nitride films are stacked on a surface of a semiconductor substrate;

forming a polysilicon film on said gate insulating film;

etching given regions of said polysilicon film and said gate insulating film to form a gate; and

performing an impurity ion implantation process to form a source region and a drain region.

Claim 2 (Previously Presented): The method of manufacturing a code address memory cell according to claim 1, wherein said gate insulating film is formed by stacking at least two or more layers of at least one of said oxide film and said nitride film.

Claim 3 (Previously Presented): The method of manufacturing a code address memory cell according to claim 1, wherein said gate insulating film has a thickness of about 30 ~ 300Å.

Claim 4 (Previously Presented): The method of manufacturing a code address memory cell according to claim 1, wherein said gate insulating film is formed by stacking a first oxide film, a nitride film and a second oxide film.

Claim 5 (Previously Presented): The method of manufacturing a code address memory cell according to claim 1, wherein said gate insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film and a second nitride film.

Claim 6 (Previously Presented): The method of manufacturing a code address memory cell according to claim 1, wherein said gate insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film.

Claim 7 (Currently Amended) A method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of:

forming a device isolation film in a given region on a semiconductor substrate to define an active region and a device isolation region;

defining said active region into a cell region and a peripheral circuit region by a given process;

forming a tunnel oxide film and a first polysilicon film on the entire structure and then patterning said tunnel oxide film and said first polysilicon film so that said tunnel oxide film and said first polysilicon film can only remain in a given region of said cell region, thus defining a floating gate;

forming an insulating film in which an oxide film and a nitride film are stacked on the entire structure ~~to form~~ and forming a second polysilicon film on the insulating film;

patterning said second polysilicon film and said insulating film so that they can remain only in a given region of said cell region and said peripheral circuit region, thus forming a control gate on the floating gate in said cell region, and a gate on a surface of the substrate in said peripheral circuit region; and

performing an impurity ion implantation process for a given region of said semiconductor substrate to form a source region and a drain region, so that a flash memory cell is formed in said cell region, and a code address memory cell is formed ~~is~~ in said peripheral circuit region.

Claim 8 (Previously Presented): The method of manufacturing a code address memory cell according to claim 7, wherein said insulating film is formed by stacking at least two or more layers of at least one of said oxide film and said nitride film.

Claim 9 (Previously Presented): The method of manufacturing a code address memory cell according to claim 7, wherein said insulating film has a thickness of about 30 ~ 300Å.

Claim 10 (Previously Presented): The method of manufacturing a code address memory cell according to claim 7, wherein said insulating film is formed by stacking a first oxide film, a nitride film and a second oxide film.

Claim 11 (Previously Presented): The method of manufacturing a code address memory cell according to claim 7, wherein said insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film and a second nitride film.

Claim 12 (Previously Presented): The method of manufacturing a code address memory cell according to claim 7, wherein said insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film.